

# **Case Study**

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# **Design of a Cortex M3 Based Security Authentication SoC**

## **Project/Client Details**

- Cortex M3 based Security authentication chip with real time boot decryption engine, battery backed up tamper protection unit and USB based finger print authentication interface
- This program was done for a *Tier 1 Semiconductor Company*

## Highlights

#### **Execution Highlights**

- Low Power SoC
- Multiple power mode support
- Multiple Voltage domain
- Memory retention
- Clock fault monitor and switching schemes

### **Design Scope**

- SoC integration and system IP design
- IO Mux Design
- Bridge IP design
- Low power implementation
- LINT, CDC, Conformal checks
- Synthesis and Post Layout STA
- Working closely with PD and DFT team till tape-out

#### Tools

SV-UVM, NCSIM, Conformal LP





# **THANK YOU**



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